High-speed and low dark current silicon-waveguide-coupled III-V photodetectors selectively grown on SOI

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Seamlessly integrating III-V active devices with Si passive components in a monolithic manner is the key for fully integrated Si photonics. In this article, we demonstrate high-performance III-V photodetectors directly grown on industry-standard (001)-oriented silicon-on-insulator (SOI) wafers and intimately coupled with Si waveguides. The Si-waveguide-coupled III-V photodetectors feature a low dark current of 60 pA corresponding to a current density of 0.002 A/cm^2, a large photocurrent exceeding 1 mA, responsivities of 0.4 A/W at 1.3 μm and 0.2 A/W at 1.5 μm, and a large detection wavelength range over the entire telecom band. High-speed measurements reveal a 3 dB bandwidth over 52 GHz and a data communication rate of 112 Gb/s with four-level pulse-amplitude modulation and 100 Gb/s with on–off keying. The monolithic integration scheme demonstrated for III-V photodetectors in this work is also applicable to future seamless integration of III-V lasers on the Si-photonics platform. © 2022 Optica Publishing Group under the terms of the Optica Open Access Publishing Agreement

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1. INTRODUCTION

With the continuing exponential growth of Internet data traffic, there is a strong economic drive to develop the technologies for low-cost, high-performance photonic integrated circuits (PICs) that can enable the continued growth of data transmission with the optical interconnect capacities of longer reach optical fiber communications networks in data centers. Emerging consumer-oriented applications such as automobiles and sensors for robotic platforms are also providing the impetus for the development of energy-efficient, densely integrated, and cost-effective PICs. Silicon photonics (Si photonics) is widely accepted as the scalable PIC platform that can address the needs for high-speed and power-efficient communications, with the pathway for low-cost dense integration offered by complementary metal oxide semiconductor (CMOS) foundries [1–6]. While Si has been employed to make excellent waveguides and high-speed modulators [7–9], the light emission and detection functionalities necessitate the integration of other materials such as germanium-on-silicon or III-V compound semiconductors [10–15]. Heterogeneous integration approaches such as wafer-bonding and micro-transfer printing have enabled the integration of high-performance III-V lasers and photodetectors on Si-photonics platforms via evanescent coupling strategies [16–18]. However, the cost and yield of manufacturing is less optimum than monolithic integration, and the large footprint of evanescent coupling limits the scalability of this approach. Monolithic integration of III-V lasers and photodiodes on Si via direct hetero-epitaxy could further benefit Si photonics in terms of cost, scalability, and integration density. In the past few years, III-V quantum dot lasers and photodetectors have been grown on Si using direct blanket hetero-epitaxy, and their performance is comparable to those grown on native III-V substrates [19–23]. Unfortunately, the micrometers thick buffer layers necessary for defect engineering severely impede the light interfacing between the III-V active devices and the passive Si elements underneath. As an alternative, selective hetero-epitaxy of III-V alloys on Si using the aspect ratio trapping (ART) technique enables closer placement and hence more efficient light coupling between the device-quality III-V gain material and the Si waveguides. Nevertheless, the epitaxial III-V material volume is often limited at nanometer scale using the ART method, which limits the output power of lasers and the photocurrent of photodetectors [24–32]. To solve this dilemma, we have implemented an integration scheme named lateral aspect ratio trapping (LART) and demonstrated the selective growth of large-area dislocation-free InP membranes on (001) silicon-on-insulator (SOI) wafers [33,34]. This monolithic InP/SOI platform with large material volume enables lower contact resistance, improved thermal dissipation, high output power for light

emitters, and large photocurrent for photodetectors. Moreover, the co-planar configuration between the epitaxial III-V material and the Si-device layer leads to compact and efficient butt-coupling schemes. Despite being still in its infancy, the LART approach has been successfully demonstrated by high-performance optically pumped lasers and photodetectors on industry-standard SOI wafers [35,36].

Earlier research of growing III-V lasers/photodiodes on Si has been focused on improving the performance of standalone III-V devices, and light interfacing strategies between III-V devices and Si waveguides have rarely been experimentally explored. Here, building from a monolithic InP/SOI platform, we take a step forward to demonstrate high-speed and low dark current III-V photodetectors selectively grown on (001) SOI wafers and efficiently butt-coupled with Si waveguides, as illustrated by the schematic in Fig. 1. The efficient light interfacing between III-V photodetectors and Si waveguides is achieved through the in-plane placement of the epitaxial III-V material with the Si-device layer and the design of a tapered waveguide. Lateral III-V p-i-n photodetectors with various dimensions were selectively grown on the same patterned SOI wafer. The crystalline defects resulting from lattice mismatch were effectively confined at the III-V/Si interface benefiting from the defecting necking effect of the LART approach. The waveguide-coupled III-V photodetectors manifest a low dark current of 60 pA, and a responsivity of 0.4 A/W at 1.3 μm and 0.2 A/W at 1.5 μm. A large 3 dB bandwidth exceeding 52 GHz and data communication rates of over 112 Gb/s were measured. These high-performance waveguide-coupled III-V photodetectors advance the state-of-the-art of future PICs that can be manufactured with seamless monolithic integration of both III-V lasers and detectors on the common Si-photonics platform.

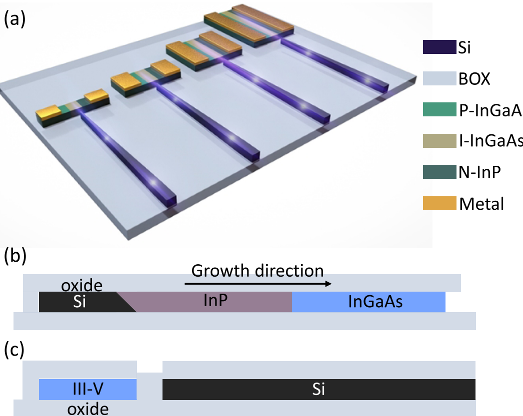

Fig. 1. (a) 3D schematic of the Si-waveguide-coupled III-V PD on SOI with various dimensions. (b) Monolithic InP/SOI platform and lateral growth of InP and InGaAs on the platform. (c) Cross-sectional view schematic illustrating the placement of III-V absorption layer and Si waveguide perpendicular to the growth direction.

2. MATERIAL GROWTH AND DEVICE FABRICATION

The waveguide-coupled photodetectors were constructed on a monolithic InP/SOI platform in a lateral configuration with various dimensions, as depicted in the 3D architecture in Fig. 1(a). The III-V materials were grown in the pre-patterned trenches using the LART approach as illustrated in Fig. 1(b) [35]. The laterally grown III-V layer situates right atop the buried oxide layer and features a co-planar configuration with the Si-device layer. The PD structure includes an unintentionally doped InGaAs layer for optical absorption and n-InP and p-InGaAs layers for ohmic contacts. The III-V are integrated with the Si in a butt-coupling scheme as depicted in the cross-sectional view schematic [Fig. 1(c)]. Starting from 8 inch commercial (001)-oriented SOI wafers, the Si-device layer was thinned down to 480 nm. The Si segments for subsequent III-V growth and waveguide definition were first defined on the Si-device layer using i-line lithography and dry etch. The Si segments for III-V lateral epitaxy were first roughly aligned with the Si segments for waveguide patterning as illustrated in Fig. 2(a). Then 600 nm thick low-temperature oxide (LTO) was deposited on the SOI wafer using low pressure chemical vapor deposition (LPCVD) and then annealed at 1000°C to densify the LTO grown at 400°C. Afterwards, 5 μm wide openings for gas diffusion supplying the

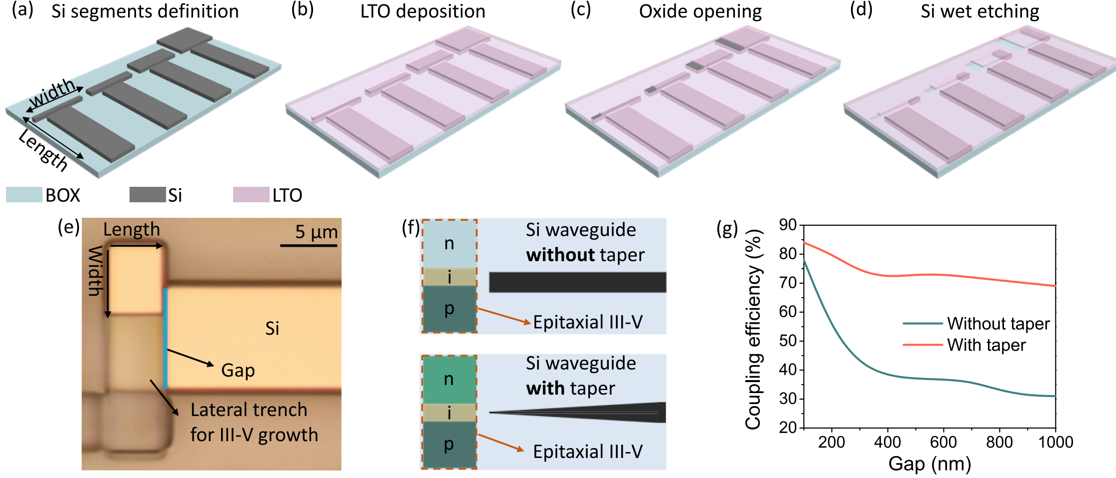

Fig. 2. (a) Definition of Si segments for III-V growth and Si-waveguide patterning. (b) LTO deposition and high-temperature annealing. (c) Oxide opening creation for sufficient gas diffusion during epitaxy. (d) Selective wet etching of Si to form the lateral trenches. (e) Patterned SOI with 7 μm wide lateral trench for III-V material growth and long Si segment for waveguide definition. (f) Top-view schematic illustrating the coupling schemes using direct butt-coupling and Si inverse taper. (g) Simulated coupling efficiency between the Si waveguide and III-V photodetector for the designed coupling scheme with and without a Si inverse taper. Taper length, 100 μm; tip width, 150 nm; thickness of the waveguide, 480 nm; waveguide width, 500 nm.

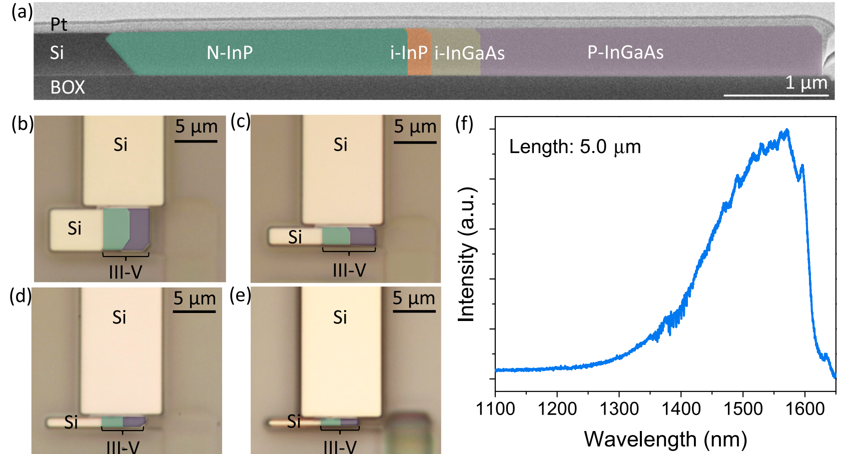

Fig. 3. (a) Color-enhanced cross-sectional view SEM image of the as-grown lateral p-i-n structure on SOI. (b)–(f) Color-enhanced optical images of as-grown p-i-n structures with III-V length of (b) 5.0 μm, (c) 2.0 μm, (d) 1.0 μm, and (e) 0.5 μm. (f) Room temperature PL of the InGaAs tested from the photodetector with 5.0 μm length.

metalorganic precursors were created on top of the segments for III-V lateral hetero-epitaxy. Finally, the lateral trenches guiding III-V growth were formed by selective wet etching of Si undercuts using KOH-based solution [Fig. 2(d)]. Figure 2(e) shows the optical image of the finished patterned SOI for growth. The narrow gap between the lateral trenches for III-V growth and the Si segment for waveguide definition is the gap between the III-V PD and Si waveguide as shown in Fig. 2(e) (labeled blue). The gap was designed to be around 400 nm, considering the limitation of the lithography and the wet etching selectivity between Si and oxide during the lateral trench creation. To minimize the multireflections through the gap and maximize the coupling efficiency between the III-V and Si, we incorporate the design of inverse tapers for the Si waveguides. The comparison of coupling schemes using direct butt-coupling and Si inverse taper is delineated in Fig. 2(f). The coupling efficiency between the III-V PD and Si waveguide with and without the Si inverse taper at various gaps was further investigated by simulation as summarized in Fig. 2(g). The dimensions of the taper design were set as follows: 100 μm taper length, 150 nm wide tip considering the fabrication capability and coupling efficiency between the waveguides and PDs, 500 nm wide for single-mode operation, and 480 nm thick waveguide, which is identical to that of the III-V PDs. Experimental demonstration was based on the same simulated dimensions. Incorporating the inverse taper structure for mode expansion enhanced mode overlap between waveguide and PD by more than two times (see Supplement 1 for more discussion), and enabled the coupling between III-V and Si to attain a high coupling efficiency of around 70% despite the relatively large gap of up to 1.0 μm. As the coupling design can also be applied to waveguide-coupled lasers on the same platform, the large tolerance on the gap will facilitate the manufacturability of this design. Aiming for PDs with a large 3 dB bandwidth, lateral trenches with identical width and different lengths spanning from 0.5 μm to 5.0 μm were included on the patterned SOI, and the III-V epitaxy is performed in a single growth run. N-InP, i-InP, i-InGaAs, and p-InGaAs were grown in sequence in the lateral trenches. The width of n-InP, i-InP, i-InGaAs, and p-InGaAs is around 2.5 μm, 150 nm, 400 nm, and 2.8 μm, respectively, and the total width of the III-V varies from 5.2 μm to 5.7 μm depending on the III-V length. As the PDs with various designed lengths were grown in the same run, somewhat smaller width was observed on the shorter PDs due to a slightly slower growth rate as a result of the smaller oxide opening. Figure 3(a) displays a cross-sectional view SEM image of the as-grown p-i-n structure with 5.7 μm epitaxial width and a 5.0 μm length defined initially by patterning. The Pt was only deposited on this PD to avoid damage during focused ion beam (FIB) cutting. The sharp InP/InGaAs interface and the transmission electron microscope (TEM) images along and perpendicular to the growth direction (see Fig. S2) suggest a high crystalline quality of the grown III-V due to the defect necking effect (see Supplement 1 for details). Figures 3(b)–3(e) display the color-enhanced optical images of the as-grown p-i-n structures with different lengths from 0.5 μm to 5.0 μm alongside the Si segments for waveguide definition. Room temperature photoluminescence (PL) from the III-V photodiodes with a length of 5.0 μm is presented in Fig. 3(f). The peak of the PL spectrum is located at around 1.5 μm, and the sharp drop at 1.6 μm is due to the cutoff of the InGaAs detector used in the PL measurement system. Lateral III-V PDs were first fabricated on the as-grown sample following the steps of oxide etching, planarization, etch back, and metallization (refer to Supplement 1, Fig. S4, for details). Note that we optimized the planarization and etch-back process and the position of the metals for lower dark current and higher speed (see Supplement 1 for more discussion). The sample was pre-treated by O_2 plasma before planarization layer coating and then cured in N_2 atmosphere after coating to achieve a clean III-V surface without residue after the etch-back process. After the fabrication of III-V PDs, the tapered Si waveguides were defined on the Si segments by E-beam lithography and a subsequent Si dry etching step. Finally, we fabricate the waveguides into edge couplers instead of grating couplers to eliminate the limitation of probing wavelength (see Supplement 1, Fig. S4).

A top-view SEM image of the fabricated Si-waveguide-integrated photodetector is shown in the optical image in Fig. 4(a). The zoomed-in coupling region including a Si taper and an III-V PD is presented in Fig. 4(b). The vertical alignment was assured by the identical thickness of the III-V PDs and Si waveguides on the same plane. The requirement of lateral alignment can be easily satisfied with the taper design and sufficient III-V device volume. The tip of the Si waveguide was roughly aligned with the

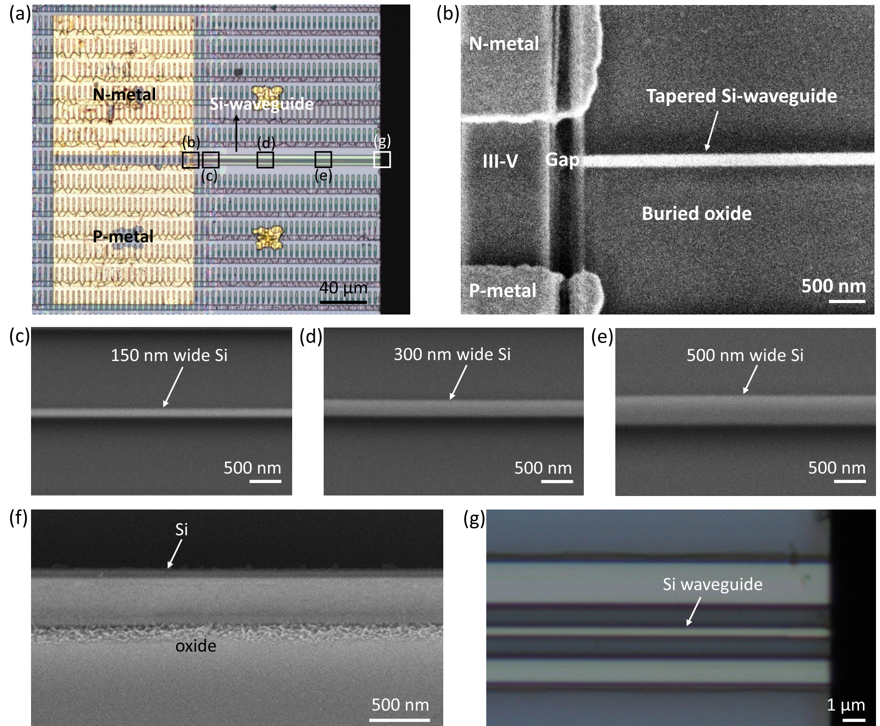

Fig. 4. (a) Top-view optical image of the finished Si-waveguide-integrated photodetector including III-V PD, tapered Si waveguide, and edge coupler. (b) Top-view SEM image illustrating the coupling of the Si waveguide and III-V PD in the same plane. (c)–(e) SEM image of tapered Si waveguide at (c) narrowest, (d) middle, and (e) widest regions. (f) Side-view SEM image of the waveguide showing smooth sidewall. (g) Top-view optical image of the edge coupler for coupling between fiber and on-chip device.

interface of InP and InGaAs to maximize absorption by the InGaAs region and minimize the loss induced by metal contacts. The narrowest, middle, and widest regions of the tapered waveguide are displayed in the zoomed-in SEM images in Figs. 4(c)–4(e), which are 150 nm, 300 nm, and 500 nm wide, respectively. The tapered Si waveguides featuring a smooth sidewall as shown in the tilted-view SEM image [Fig. 4(f)] ensure a low propagation loss. The edge couplers with flat end facets were fabricated through polishing for the coupling from fiber to Si waveguide as illustrated in the optical image in Fig. 4(g).

3. RESULTS AND DISCUSSION

We first carried out static characterizations of the fabricated Si-waveguide-coupled PDs. Benefiting from the unique design and high quality of III-V material, a low dark current of 60 pA was achieved for the PD biased at −1 V. The dark current density was calculated to be 0.002 A/cm^2, normalized to the cross section of the p-i-n diode. Compared with our previously reported III-V PDs using the vertical ART approach, the dark current of the waveguide-integrated PDs was three orders of magnitude lower [27]. This reduction is a combined result of the elimination of the defective InP/Si interface in the current path, the high crystalline quality of epitaxial III-V material, and passivation at sidewalls enabled by the optimal planarization and etch-back process. And this value is comparable with the lowest dark current reported for PD grown on thick III-V buffers on Si [21].

The measured temperature dependence of the dark current from room temperature to elevated temperatures up to 95°C [Fig. 5(a)] demonstrates the capability of the devices for operation at high temperatures. Specifically, the dark current at −1 V is less than 1 nA even when the temperature is raised up to 85°C. The corresponding current density ranges from 0.002 to 0.03 A/cm^2 between 25°C and 95°C (see Supplement 1 and Fig. S5 for more details). To characterize the photoresponse in the telecom band, excitation light in the O band and C band was coupled into the Si waveguide at the edge through a fiber with a measured coupling loss of 10 dB, and the generated photocurrent was measured by a source meter. The optical field from the Si waveguide was coupled to the III-V PD through the 400 nm air gap. Figure 5(b) plots the dark current and photocurrent of a 1.0 µm long device under the illumination of 1310 nm and 1550 nm sources at reverse biases from −2 V to 0 V. With incident power of around 1 µW, an obvious photocurrent can be measured, which is evidence of the high sensitivity of the PDs. The comparable sensitivity achieved through the Si waveguide and top illumination in free space suggests a high coupling efficiency between the Si waveguides and III-V PDs. For all the measured devices, the photocurrent at 1310 nm is higher than that at 1550 nm, which might be due to stronger absorption at shorter wavelengths [37,38]. The responsivity at 1.3 µm and 1.5 µm was calculated to be 0.4 A/W and 0.16 A/W without accounting for the coupling loss between the Si waveguides and III-V PDs, respectively. We also investigated the incident power and bias dependence of the photoresponse by illuminating the PD through the Si waveguide with elevated excitation powers and recorded the corresponding photocurrents at various biases from −3 V to 0 V [Fig. 5(c)]. The photocurrent increased linearly with the elevated excitation power, and no obvious dependence on the bias was observed, suggesting a

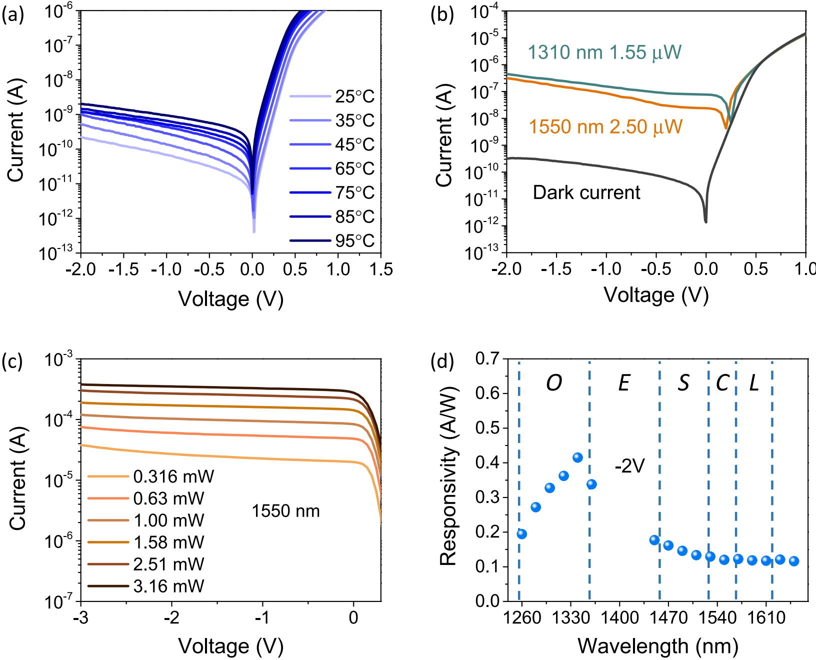

Fig. 5. (a) Temperature-dependent dark current of the PD with 0.5 μm length from 25°C to 95°C. (b) Dark current and photocurrent at 1310 nm and 1550 nm for a device with 1.0 μm length showing the high sensitivity. (c) Power-dependent photocurrent measured at 1550 nm for the device with 1.0 μm length. (d) Responsivity at various probing wavelengths from 1260 nm to 1650 nm.

large saturation current, low operating bias, and trap-free characteristics (refer to Supplement 1 for more details). The PD had a saturation photocurrent of more than 1 mA at 1550 nm. The large photocurrent and high sensitivity indicate low energy consumption and high efficiency of the waveguide-coupled PDs. As the PDs can operate in both the O band and the C band, we further investigate the operation wavelength range by measuring the PDs from 1260 nm to 1650 nm. Figure 5(d) shows the responsivity measured from a 1 μm long device at various wavelengths with a span of around 400 nm covering the O, E, S, C, and L bands, which matches the spectral range typically used in optical fiber communications. The responsivity first peaked to 0.44 A/W at 1.3 μm and gradually decreased to 0.12 A/W at 1.6 μm showing no dependence on the bias for all the wavelengths measured. The missing data from 1370 nm to 1450 nm is due to the limited tuning range of tunable lasers used in the measurement. The responsivity after the normalization of the 70% coupling efficiency between the Si waveguide and III-V PD is calculated to be 0.6 A/W at 1.3 μm and 0.2 A/W at 1.5 μm, respectively. The responsivity of the waveguide-coupled PDs with different dimensions is comparable within a 0.05 A/W margin, while the saturation photocurrent increases with the device length due to the better thermal dissipation of larger devices after an extended period of continuous wave (CW) laser excitation. The true material responsivity should be higher than the values shown here as the unknown metal-induced optical losses, which are non-negligible in this structure, have not been included. Forming a ridge with shallow etch of the p-InGaAs and n-InP at the InGaAs absorbing region could improve the responsivity as well.

For the dynamic characterizations, we first investigated the 3 dB bandwidth of the waveguide-coupled PDs through impulse-response measurements (refer to Supplement 1, Fig. S7a, for more details). The optical signal generated by a femtosecond fiber laser at 1550 nm was coupled to the Si-waveguide-coupled III-V PDs under test. A 45 GHz bias tee was used to combine the DC and RF signals, and the output signal was observed on the sampling oscilloscope. An electrical pulse with ∼9 ps full width at half maximum (FWHM) was measured from the Si-waveguide-coupled

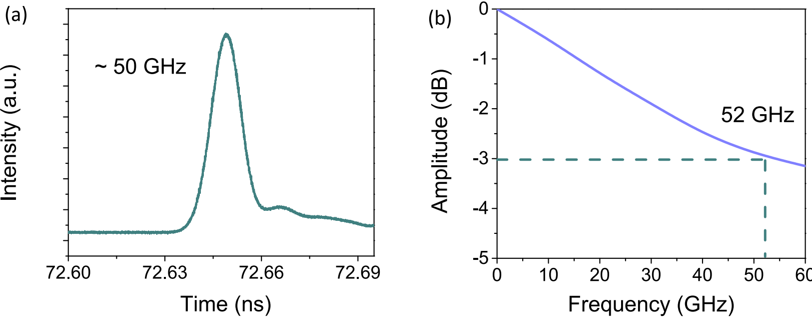

Fig. 6. (a) Output electrical pulse measured from the device with 1.0 μm length through the impulse-response method. (b) Frequency response obtained by Fourier transform with an extracted 3 dB bandwidth of 52 GHz.

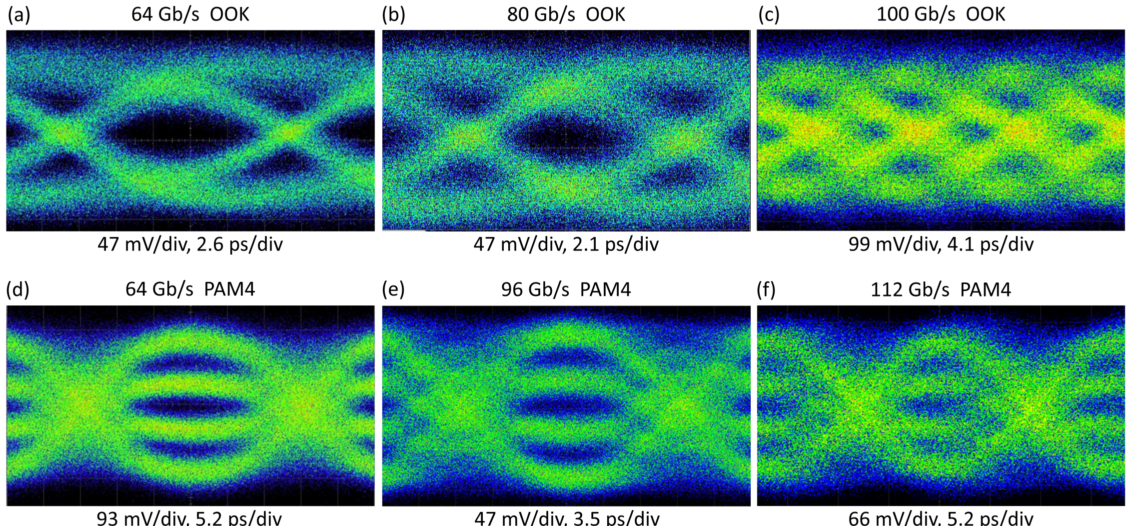

Fig. 7. (a) 64 Gb/s, (b) 80 Gb/s, and (c) 100 Gb/s OOK eye diagram under −2 V bias. (d) 64 Gb/s, (e) 96 Gb/s, and (f) 112 Gb/s PAM4 eye diagram measured at −2 V.

III-V PD with a PD length of 1.0 μm when biased at −2 V as shown in Fig. 6(a). The 3 dB bandwidth is calculated to be 50 GHz for the measured pulse with Gaussian shape according to the time-bandwidth product $\Delta f \cdot \Delta t = 0.441$, where Δf is the 3-dB bandwidth of the photodetector, and Δt is the FWHM of the output pulse. We also performed Fourier transform to confirm the 3 dB bandwidth of the device [39]. The result shows a 3 dB bandwidth of 52 GHz as presented in Fig. 6(b). The junction capacitance was calculated to be around 0.7 fF, and the resistance was extracted to be around 1.5 kΩ. The RC limited bandwidth was estimated to be 190 GHz, and the transit time limited bandwidth was calculated to be 74 GHz, both of which are higher than the measured value. As we only consider the RC and transit time limit in our calculations, we assume that at a bias of −2 V the minority-carrier diffusion is not a dominant limiting factor for 3 dB bandwidth. As the waveguide-integrated PDs with various dimensions and at various biases show similar results on the 3 dB bandwidth, it is likely that the 3 dB bandwidth is still limited by the temporal resolution of the sampling oscilloscope and the bandwidth of the electrical probes used in the measurement setup with an upper limit similar to the measurement result. The viability of the waveguide-integrated PD was confirmed by measuring the data transmission with on–off keying (OOK) and four-level pulse-amplitude modulation (PAM4) (see Supplement 1 and Fig. S7b for more details of the measurement). To ease the measurement we mainly performed the measurement on 5 μm long devices with higher saturation photocurrent. Figures 7(a)–7(c) depict the open electrical eye diagrams of 64 Gb/s, 80 Gb/s, and 100 Gb/s OOK for a 5 μm long device, which are demonstrated for the first time, to the best of our knowledge, for the III-V PDs monolithically integrated on Si. The eye diagrams of 64 Gb/s, 96 Gb/s, and 112 Gb/s PAM4 were also realized as displayed in Figs. 7(d)–7(f). The results indicated the high-quality data reception performance of the fabricated waveguide-coupled PDs. When measuring the waveguide-integrated PDs with various dimensions, the PDs with larger dimensions show slightly improved eye opening as they can sustain larger incident power and photocurrent. The eye diagrams were measured under a photocurrent ranging from 0.5 mA to 1.5 mA. No degradation was observed with the increasing photocurrent.

4. CONCLUSION

In conclusion, we demonstrated superior performance of monolithically integrated Si-waveguide-coupled III-V PDs on standard (001)-oriented SOI platforms. The waveguide-coupled photodetectors manifest a low dark current of 60 pA at −1 V characterized under room temperature corresponding to a current density of 0.002 A/cm^2, a responsivity of 0.4 A/W at 1.3 μm and 0.2 A/W at 1.5 μm, a saturation photocurrent over 1 mA, and an operation wavelength spanning from 1260 nm to 1650 nm. The responsivity is underestimated due to the exclusion of metal-induced loss and coupling loss and can be further improved by enlarging the width of the i-InGaAs and enhancing the optical confinement at the absorption region through etching physical structures. The detection range covers the entire telecommunication band including the O, E, S, C, and L bands. Also, a 3 dB bandwidth exceeding 52 GHz and data communication over 112 Gb/s were achieved for the PDs with various dimensions. The metal contacts can be optimized for RF performance to gain superior high-speed characteristics. The coupling efficiency of the system, estimated to be as high as 70%, was validated by the decent responsivity and high sensitivity. The coupling efficiency can be further increased by reducing the gap and filling the air gap with oxide or other dielectric material for better mode field matching. The efficient light coupling demonstrated by the Si-waveguide-coupled III-V PDs addressed the critical issue of fully integrated PIC, which has not been available by other integration methods. Furthermore, the coupling scheme is also applicable to future integration of lasers and waveguides on this platform in a simple manner without introducing large loss to the laser cavity. Various III-V devices (lasers, photodetectors, modulators, etc.) with different dimensions and Si features (resonators, gratings, waveguides, etc.) can be integrated on the same chip by modifying the design of patterned SOI wafer guiding the III-V selective growth. The high performance of the Si-waveguide-coupled III-V PDs and the robust coupling strategy prove their

capability for practical applications in optical communications and provide a promising solution for fully integrated Si photonics.

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Data availability. Data underlying the results presented in this paper are not publicly available at this time but may be obtained from the authors upon reasonable request.

Supplemental document. See Supplement 1 for supporting content.

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